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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/801,260	03/15/2004	Ichiro Fujimori	13912US04	2251

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EXAMINER	
CAO, PHAT X	
ART UNIT	**PAPER NUMBER**
2814	

MAIL DATE	DELIVERY MODE
02/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	Application No. 10/801,260	Applicant(s) FUJIMORI, ICHIRO	
	Examiner Phat X. Cao	Art Unit 2814	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 22 January 2007 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____ months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *1-15*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: see attached papers.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

ADVISORY ACTION

1. Applicant argues that the layer 12 having a higher doping than the underlying substrate 10 for providing immunity against parasitic substrate effects is not supported by McCormack.

This argument is not persuasive because as stated at column 1, lines 19-24 of McCormack:

> While a lightly doped p-type substrate having a resistivity of 5 or 20 ohm-cm has been used in early fabrication processes, this was found to be problematic for CMOS integrated circuits because the high substrate resistance renders the integrated circuit more susceptible to latchup.

From this statement, one of ordinary skill in the art would recognize that the lightly doped (p-) substrate 10 shown in Fig. 2 is found to be problematic for CMOS integrated circuits because its high resistance renders the integrated circuit more susceptible to latchup.

And at column 4, lines 9-13, McCormack states that:

> A conventional way to reduce latchup susceptibility is to lower the resistance of the P-wells. A low P-well resistance has the effect of decoupling the parasitic bipolar transistors formed by the source/drain regions and the n and p tubs in a CMOS process.

From this statement, one of ordinary skill in the art would recognize that the parasitic bipolar transistors formed by the source/drain regions and the n and p tubs in a CMOS shown in Fig. 2 are prevented by lower the resistance of the lightly doped (p-)

substrate 10. The low resistance lightly doped (p-) substrate 10 is provided by placing higher doped (p) layer 12 on top of the lightly doped (p-) substrate 10.

Applicant further argues that the (p) type layer 12 would not have higher doping than the lightly doped (p-) substrate 10 because the resistance for both the (p) type layer 12 and the lightly doped (p-) substrate 10 are in the same range of 14-28 ohm-cm.

This argument is not persuasive because as very well known to one of ordinary skill in the art, the (p) type doping would have higher doping than the (p-) type doping because the "negative" sign indicates the lower doping concentration. The examiner recognizes that McCormack discloses that the resistance for both the (p-) substrate 10 and the (p) layer 12 are in the same range of 14-28 ohm. However, it does not mean that these two layers would have the same resistance. For example, one layer can have the resistance of 15 ohm and the other layer can have higher resistance of 20 ohm. These two example layers have different in resistance but they are still in the same range of 14-28 ohm.

Applicant also argues that nowhere in the McCormack reference recites that the (p) type layer 12 is a "shielding layer". It is noted that although McCormack does not explicitly state that the (p) type layer 12 is a "shielding layer", "shielding layer" is a label that does not structurally distinguish over the (p) type layer 12 in McCormack. The (p) type layer 12 of McCormack functions as a "shielding layer" because the layer 12 shields the well layers from the substrate 10 and has a resistivity lower than the resistivity of the substrate 10 for enhancing latchup suppression. Labels, statements of intended use, or functional language do not structurally distinguish claims over the prior

art, which can function in the same manner, be labeled in the same manner, or be used in the same manner. See *In re Pearson*, *Ex parte Minks*, and *In re Swinehart*. Therefore, Applicant again has failed to provide the evidence to support that the layer 12 is not a shielding layer for reducing latchup or noise even though it shields the well layers from the high resistivity substrate and it has a resistivity lower than the resistivity of the substrate.

Regarding the combination of Wei and Puar, Applicant argues that Wei's Fig. 4 does not disclose "at least one transistor of a first transistor type that couples said transistor layer to said shielding layer" as claimed.

This argument is not persuasive because as clearly stated in the ground of rejection, "at least one transistor of a first transistor" refers to a PMOS transistor (not labeled), "said transistor layer" refers to N-well/P-well layer 46, and "said shielding layer" refers to layer 484. Clearly, the first transistor type of PMOS couples the transistor layer 46 to the shielding layer 484.

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PC

February 8, 2007

PHAT X. CAO
PRIMARY EXAMINER